WHAT IS CLAIMED IS:

1. An apparatus comprising:

a pseudo-dynamic latch; and

a deracer circuit configured to prevent a select signal from being high when a precharge edge of a data signal arrives.

2. The apparatus of claim 1, wherein the deracer circuit comprises:

a first logic gate configured to receive the data signal from a domino logic circuit and to invert the data signal; and

a second logic gate configured to receive the data signal and an inverted select signal and to generate the select signal.

3. The apparatus of claim 2, wherein the deracer circuit is configured to generate a state change of the select signal two gate delays after a state change of the data signal.

4. The apparatus of claim 3, wherein the deracer circuit is configured to prevent the select signal from going to a high state before the pseudo-dynamic latch goes into a hold state from an evaluate state.

5. The apparatus of claim 2, wherein the first logic gate is an inverter and the second logic gate is a NOR gate.

6. The apparatus of claim 1, wherein the data signal is a domino-precharge signal that is precharged to a high state.

7. The apparatus of claim 1, wherein the apparatus is at least one of a multiplexer, an Arithmetic Logic Unit (ALU), a memory and a microprocessor.

8. The apparatus of claim 1, wherein the deracer circuit comprises:

a first logic gate configured to receive an negative logic clock signal and to invert the negative logic clock signal; and

a second logic gate configured to receive the inverted negative logic clock signal and an inverted select signal and to generate the select signal.

9. The apparatus of claim 8, wherein the first and second logic gates are configured to prevent the select signal from going to a high state before a the pseudo dynamic latch goes into a hold state from an evaluate state.

10. The apparatus of claim 8, wherein the first logic gate is an inverter and the second logic gate is a NOR gate.

11. The apparatus of claim 1, wherein the deracer circuit comprises:

a logic gate configured to receive a clock signal and an inverted select signal and to generate the select signal.

12. The apparatus of claim 11, wherein the logic gate prevents the select signal from going to a high state before the pseudo-dynamic latch goes into a hold state.

13. The apparatus of claim 11, wherein the logic gate is a NOR gate.

14. A latch comprising:

a deracer circuit configured to prevent a select signal from being high when a precharge edge of a data signal arrives.

15. The latch of claim 14, wherein the deracer circuit comprises:

a first logic gate configured to receive the data signal from a domino logic circuit and to invert the data signal; and

a second logic gate configured to receive the data signal and an inverted select signal and to generate the select signal.

16. The latch of claim 15, wherein the deracer circuit is configured to generate a state change of the select signal two gate delays after a state change of the data signal.

17. The latch of claim 15, wherein the select signal and data signal are in a pull down path of the latch.

18. The latch of claim 15, wherein the first logic gate is an inverter and the second logic gate is a NOR gate.

19. The latch of claim 15, wherein the data signal is a domino-precharge signal that is precharged to a high state.

20. A method for implementing a pseudo-dynamic latch, the method comprising:

receiving a data signal from a domino logic circuit; and

preventing a select signal from being high when a precharge edge of the data signal arrives.

21. The method of claim 20, further comprising:

inverting the data signal with a first logic gate; and

receiving the inverted data signal and an inverted select signal and generating the select signal with a second logic gate.

22. The method of claim 21, further comprising:

generating a state change of the select signal two gate delays after a state change of the data signal.

23. The method of claim 22, further comprising:

preventing the select from going to a high state before the pseudo-dynamic latch goes into a hold state from an evaluate state.

24. The method of claim 21, wherein the data signal is a domino-precharge signal that is precharged to a high state.

25. The method of claim 21, wherein the first logic gate is an inverter and the second logic gate is a NOR gate.

26. A system comprising:

a microprocessor; and

an off-die component in communication with the microprocessor; wherein the microprocessor comprises a pseudo-dynamic latch including a deracer circuit, wherein the deracer circuit is configured to prevent a select signal from being high when a precharge edge of a data signal arrives.

27. The system of claim 26, wherein the deracer circuit comprises:

a first logic gate configured to receive the data signal from a domino logic circuit and to invert the data signal;

a second logic gate configured to receive the inverted data signal and an inverted select signal and to generate the select signal.

28. The system of claim 27, wherein the deracer circuit is configured to generate a state change of the select signal two gate delays after a state change of the data signal.

29. The system of claim 27, wherein the deracer circuit is configured to prevent the select signal from going to a high state before the pseudo-dynamic latch goes into a hold state from an evaluate state.

30. The system of claim 27, wherein the first logic gate is an inverter and the second logic gate is a NOR gate.